CLAIMS

1. A method of producing a carrier wafer for an integrated circuit, said method comprising the steps of:

providing a carrier wafer having a plurality of bump pads and a plurality of wire bond pads;

providing a passivation layer on said carrier wafer;

etching a passivation layer over at least a portion of said plurality of bump pads;

applying solder bumps on said plurality of bump pads; and

separately etching the passivation layer over at least a portion of said plurality of wire bond pads.

2. The method of claim 1 wherein said step of providing a carrier wafer comprises a step of providing a carrier wafer having traces connecting at least a portion of said plurality of bump pads.

3. The method of claim 2 further comprising a step of coupling a flip chip to said carrier wafer.

4. The method of claim 3 wherein said step of coupling said flip chip to said carrier wafer comprises a step of coupling said flip chip to another flip chip by way of said traces on said substrate.

5. The method of claim 1 further comprising a step of providing wire bonds between said plurality of wire bond pads and a plurality of wire bond pads on a substrate.

6. A method of producing a carrier wafer for an integrated circuit, said method comprising the steps of:

providing a passivation layer over a plurality of bump pads and a plurality of wire bond pads formed on a carrier wafer;

etching said passivation layer over at least a portion of said plurality of bump pads;

applying solder bumps on said plurality of bump pads;

separately etching the passivation layer over at least a portion of said plurality of said wire bond pads; and

coupling a flip chip to said plurality of bump pads.

7. The method of claim 6 further comprising a step of providing traces connecting at least some of said plurality of bump pads on said carrier wafer.

8. The method of claim 7 wherein said step of coupling a flip chip to said plurality of bump pads comprises a step of coupling said flip chip to another flip chip by way of said traces.

9. The method of claim 8 further comprising a step of connecting programmable logic of said flip chip to programmable logic of said other flip chip.

10. The method of claim 6 further comprising a step of providing a wire bond between said plurality of wire bond pads and a plurality of wire bond pads on a substrate.

11. A method of producing a carrier wafer for an integrated circuit, said method comprising the steps of:

providing a silicon carrier wafer having a plurality of bump pads connected by a plurality of traces, and a plurality of wire bond pads;

providing a passivation layer over said plurality of bump pads and said plurality of wire bond pads;

etching said passivation layer over said plurality of bump pads;

applying solder bumps on said plurality of bump pads;

separately electing said passivation layer over said plurality of wire bond pads; and

coupling a plurality of flip chips to said plurality of bump pads.

12. The method of claim 11 comprising a step of connecting a region of a first flip chip to a region of a second flip chip.

13. The method of claim 12 wherein said step of connecting a region of a first flip chip to a region of a second flip chip comprises a step of connecting programmable logic of said first flip chip and said second flip chip.

14. The method of claim 11 further comprising a step of providing a wire bond between a wire bond pad of said plurality of wire bond pads and a wire bond pad of a substrate.

15. A method of producing a carrier wafer for an integrated circuit, said method comprising the steps of:

providing a silicon carrier wafer having a plurality of bump pads connected by a plurality of traces and a plurality of wire bond pads;

providing a passivation layer on said plurality of bump pads and said plurality of wire bond pads;

etching said plurality of bump pads;

applying solder bumps on said plurality of bump pads;

separately electing said passivation layer over said plurality of wire bond pads after applying said solder bumps;

positioning a plurality of flip chips on said plurality of bump pads;

coupling said carrier wafer to a substrate;

providing a plurality of wire bonds between said plurality of wire bond pads and a plurality of wire bond pads on said substrate;

applying an encapsulation layer over said flip chips and said plurality of wire bonds;

applying a plurality of solder balls to said substrate; and

attaching a metal lid over said substrate.

16. An integrated circuit employing a flip chip, said integrated circuit comprising:

a carrier wafer having a plurality of bump pads and a plurality of wire bond pads;

a passivation layer formed on said carrier wafer over said plurality of bump pads and a plurality of wire bond pads;

a solder bump formed on a bump pad within a first etched window in said passivation layer, said first etched window being formed in a first etching step; and

a second etched window over at least a portion of said wire bond pad, said second etched window being formed in said passivation layer by a second etching step.

17. The integrated circuit of claim 16 wherein said carrier wafer comprises a plurality of traces connecting at least some of said plurality of bump pads.

18. The integrated circuit of claim 17 further comprising a plurality of flip chips coupled to said carrier wafer.

19. The integrated circuit of claim 18 wherein some of said plurality of flip chips are coupled by way of said traces.

20. The integrated circuit of claim 16 further comprising a plurality of wire bonds coupled to at least some of said wire bond pads.

21. An integrated circuit employing a flip chip, said integrated circuit comprising:

a carrier wafer having a plurality of bump pads and a plurality of wire bond pads;

a solder bump formed on a bump pad within a first etched window in a passivation layer, said first etched window being formed in a first etching step;

a second etched window over at least a portion of said wire bond pad, said second etched window being formed in said passivation layer by a second etching step;

a substrate receiving said carrier wafer; and

a plurality of wire bonds providing a connection between said plurality of wire bond pads and a plurality of wire bond pads on said substrate.

22. The integrated circuit of claim 21 further comprising a plurality of flip chips coupled to said carrier wafer.

23. The integrated circuit of claim 21 further comprising an encapsulation layer covering said plurality of flip chips and said plurality of wire bonds.

24. The integrated circuit of claim 23 further comprising a metal lid enclosing said encapsulation layer.

25. The integrated circuit of claim 21 further comprising a comprising a plurality of solder balls on said substrate.